REMARKS/ARGUMENTS

Claims 2-10 and 12-20 are currently pending in the present patent application.

In Section 5 of the Final Office Action mailed on July 28, 2008, in the above-referenced patent application, the Examiner objects to the specification because the title of the invention refers to a "bidimensional accessible memory"; however, the claims, for instance independent claim 1, are directed to a "monodimensional accessible memory". The "Pseudo Bidimensional Randomly Accessible Memory" is considered to be accurate since, for example, in claim 3, when operating in the second configuration although the sub-arrays function as monodimensional blocks or memory the sub-arrays collectively function to provide bidimensional or random access to the memory locations. The term "pseudo" indicates that the functionality if that of a bidimensional memory while the specific structure of each sub-array is monodimensional. If the Examiner still objects to the title the undersigned will be happy to amend the title to the satisfaction of the Examiner.

In Section 6 of the Final Office Action, the Examiner objects to claims 8 and 14 due to grammatical informalities and antecedent basis issues. Claims 8 and 14 have been amended to correct these nonsubstantive errors.

In Section 8 of the Final Office Action, the Examiner rejects claims 8-10 and 12-20 under 35 USC § 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Particularly, claims 8, 12, 14, and 15 recite inter alias "...the same predetermined one of the memory locations is used to allow sequential access to the contents of the memory locations... or ...allow access to a same predetermined one of the memory locations..." This language was added merely in an attempt to distinguish the subject matter recited by these claims and disclosed in the application from the prior art. This language has been removed through the above claim amendments.

In Section 10 of the Final Office Action, the Examiner rejects claims 8-10 and 14-16 under 35 USC § 102(e) as being anticipated by US Patent Publication No. 2002/0087817 to Tomaiuolo ("Tomaiuolo").

Amended claim 8 recites a memory including a plurality of memory locations and a control circuit coupled to the memory locations and operable to allow random access to the memory locations during a read mode of operation and allow sequential access to the memory locations during a write mode of operation. Tomaiuolo does not disclose such a memory that provides random access to memory locations during read operations while providing sequential access to memory locations during write operations. In Tomaiuolo the sequential or random access in Tomaiuolo is determined not based upon whether the operation is a read or write operation but is based upon the addresses of the memory locations being accessed. Thus, Tomaiuolo does not disclose or suggest providing random access to memory locations during read accesses and sequential access during write accesses.

For at least these reasons, the combination of elements recited in claim 8 is allowable. Dependent claims 9 and 10 are allowable for at least the same reasons as claim 8 and due to the additional limitations added by each of these dependent claims. Claims 14-16 are allowable for reasons similar to those just set forth with regard to claim 8.

In Section 12 of the Final Office Action, the Examiner rejects claims 1-7 under 35 USC § 103(a) as being unpatentable over US Patent No. 6,091,645 to Iadanza ("Iadanza") in view of Applicant Admitted Prior Art ("APA").

Independent claim 3 recites, in part, a memory including at least one array of memory elements and a partition of the at least one array into a plurality of sub-arrays of the memory elements and an array configuration circuit for selectively putting the at least one array in one of two operating configurations. The first operating configuration is a data storage configuration in which the memory is put when data are

to be stored therein and the second operating configuration is a data retrieval configuration in which the memory is put when data are to be retrieved therefrom.

While Iadanza discloses a memory that can be configured to operate in various modes, such as RAM, FIFO, and LIFO (see col. 2, lines 28-36), each sub-array12 (Figure 1A) is "programmed into, and thereafter accessed using, one of a set of modes." Id. Nowhere does Iadanza disclose or suggest operating in different modes based upon whether the access of the memory is a read or write operation. Each sub-array is configured to operate in a set mode, and this mode does not vary depending upon whether the sub array is being accessed for a read or a write operation.

For at least these reasons, the combination of elements recited in claim 3 is allowable. Dependent claims 2 and 4-7 are allowable for at least the same reasons as claim 3 and due to the additional limitations added by each of these dependent claims.

In Section 13 of the Final Office Action, the Examiner rejects claims 12-13 and 17-20 under 35 USC § 103(a) as being unpatentable over Tomaiuolo in view of APA and further in view of Iadanza.

Amended claim 12 recites a memory including an array of memory locations; and a control circuit coupled to the array and operable to cause the array to operate as a random-access memory during a read mode of operation and a first-in-first-out memory during a write mode of operation. The memory locations comprise rings of serially coupled memory locations, each having a respective contents, with the contents of each ring being independent of the contents of the other rings. During the read mode of operation, the control circuit is operable to control each of the rings to receive a clock signal, shift the contents of each respective memory location in the ring to a respective next memory location in the ring once per cycle of the clock signal, and allow access to one of the memory locations during a predetermined cycle of the clock signal. The portion of the cited APA (para. 6) merely discloses a FIFO memory and as is the case such a memory is not limited to read or write accessed can be both written to and read from.

The combination of the these three references and the teachings thereof simply do not disclose or suggest operating memory locations in one way during read accesses and in other way during write accesses. The same is true of the Tomaiuolo and Iadanza references, namely neither discloses nor suggests operating as a random access memory during reads and a FIFO during writes. For at least these reasons, the combination of elements recited in claim 12 is allowable. Dependent claim 13 is allowable for at least the same reasons as claim 12 and due to the additional limitations added by this dependent claim. Claims 17-20 are allowable for reasons similar to those just discussed above with regard to claim 12.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **Should the Examiner have any further questions about the application, Applicants respectfully request the Examiner to contact the undersigned attorney at (425) 455-5575 to arrange for a telephone interview to discuss the outstanding issues.** If the need for any fee in addition to any fee paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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